Your search matched **48** of **804507** documents.
Results are shown **15** to a page, sorted by **publication year** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the text box.

Then click **Search Again**.

(multiplier <and> selection <and> adder)

Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **A carry-select-adder optimization technique for high-performance booth-encoded wallace-tree multipliers**
Liao, M.-J.; Su, C.-F.; Chang, C.-Y.; Wu, A.C.-H.
Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on , Volume: 1 , 2002
Page(s): 81 -84

[Abstract] [PDF Full-Text (444 KB)] **CNF**

2 **A power minimization technique for arithmetic circuits by cell selection**
Muroyama, T.; Ishihara, T.; Hyodo, A.; Yasuura, T.
Design Automation Conference, 2002. Proceedings of ASP-DAC 2002. 7th Asia and South Pacific and the 15th International Conference on VLSI Design. Proceedings. , 2002
Page(s): 268 -273

[Abstract] [PDF Full-Text (628 KB)] **CNF**

3 **Design of synchronous and asynchronous variable-latency pipelined multipliers**
Olivieri, M.
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 9 Issue: 2 , April 2001
Page(s): 365 -376

[Abstract] [PDF Full-Text (344 KB)] **JNL**

4 **32-bit constant (k) coefficient multiplier**

Al-Khalili, A.J.; Zaman, N.-U.
Electrical and Electronic Technology, 2001. TENCON. Proceedings of IEEE Region 10 International Conference on , Volume: 1 , 2001
Page(s): 306 -308 vol.1

[Abstract] [PDF Full-Text (240 KB)] **CNF**

---

5 **1 GHz HAL SPARC64/sup R/ Dual Floating Point Unit with RAS features**
Naini, A.; Dhablania, A.; James, W.; Das Sarma, D.
Computer Arithmetic, 2001. Proceedings. 15th IEEE Symposium on , 2001
Page(s): 173 -183

[Abstract] [PDF Full-Text (1280 KB)] **CNF**

---

6 **Using carry-save adders in low-power multiplier blocks**
Bartlett, V.A.; Dempster, A.G.
Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on , Volume: 4 , 2001
Page(s): 222 -225 vol. 4

[Abstract] [PDF Full-Text (268 KB)] **CNF**

---

7 **Design of a high performance 32/spl times/32-bit multiplier with a novel sign select Booth encoder**
Kiwon Choi; Minkyu Song
Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on , Volume: 2 , 2001
Page(s): 701 -704 vol. 2

[Abstract] [PDF Full-Text (368 KB)] **CNF**

---

8 **A multicarrier QAM modulator**
Vankka, J.; Kosunen, M.; Sanchis, I.; Halonen, K.A.I.
Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on , Volume: 47 Issue: 1 , Jan. 2000
Page(s): 1 -10

[Abstract] [PDF Full-Text (224 KB)] **JNL**

---

9 **A QAM modulator for WCDMA base station**
Vankka, J.; Sumanen, L.; Halonen, K.
ASIC/SOC Conference, 2000. Proceedings. 13th Annual IEEE International , 2000

Page(s): 65 -69

[Abstract] [PDF Full-Text (376 KB)] **CNF**

10 **A compact adaptive equalizer IC for HIPERLAN system**
Jinn-Shyan Wang; Pei-Lung Lin; Wern-Ho Sheen; Duo Sheng; Yu-Ming Huang
Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on , Volume: 2 , 2000
Page(s): 265 -268 vol.2

[Abstract] [PDF Full-Text (360 KB)] **CNF**

11 **Multiple low swing voltage values for CPL, CVSL and domino logic families**
Rjoub, A.; Koufopavlou, O.
Electronics, Circuits and Systems, 2000. ICECS 2000. The 7th IEEE International Conference on , Volume: 2 , 2000
Page(s): 903 -906 vol.2

[Abstract] [PDF Full-Text (256 KB)] **CNF**

12 **A programmable FIR filter using serial-in-time multiplication and canonic signed digit coefficients**
Kosunen, M.; Halonen, K.
Electronics, Circuits and Systems, 2000. ICECS 2000. The 7th IEEE International Conference on , Volume: 1 , 2000
Page(s): 563 -566 vol.1

[Abstract] [PDF Full-Text (268 KB)] **CNF**

13 **Low-power circuit implementation for partial-product addition using pass-transistor logic**
Law, C.F.; Rofail, S.S.; Yeo, K.S.
Circuits, Devices and Systems, IEE Proceedings- , Volume: 146 Issue: 3 , June 1999
Page(s): 124 -129

[Abstract] [PDF Full-Text (564 KB)] **JNL**

14 **High-level synthesis of power-optimized and area-optimized circuits from hierarchical data-flow intensive behaviors**
Lakshminarayana, G.; Jha, N.K.
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 18 Issue: 3 , March 1999

Page(s): 265 -281

[Abstract] [PDF Full-Text (388 KB)] **JNL**

15 **A joint gate sizing and buffer insertion method for optimizing delay and power in CMOS and BiCMOS combinational logic**

Lowe, K.S.; Gulak, P.G.

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 17 Issue: 5 , May 1998

Page(s): 419 -434

[Abstract] [PDF Full-Text (508 KB)] **JNL**

1 2 3 4 [Next]

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search
Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting
No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ| Terms | Back to Top

Your search matched **48** of **804507** documents.
Results are shown **15** to a page, sorted by **publication year** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the text box.

Then click **Search Again**.

(multiplier <and> selection <and> adder)

Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

16 **Accuracy sensitive word-length selection for algorithm optimization**
Wadekar, S.A.; Parker, A.C.
Computer Design: VLSI in Computers and Processors, 1998. ICCD '98. Proceedings. International Conference on , 1998
Page(s): 54 -61

[Abstract] [PDF Full-Text (132 KB)] **CNF**

17 **Synthesis of power-optimized and area-optimized circuits from hierarchical behavioral descriptions**
Lakshminarayana, G.; Jha, N.K.
Design Automation Conference, 1998. Proceedings , 1998
Page(s): 439 -444

[Abstract] [PDF Full-Text (672 KB)] **CNF**

18 **A high-speed of self-timing carry-completion for direct two's complement multipliers**
Hao-Yung Lo; Sha-Fen Ling; Chun-Ming Shie
Circuits and Systems, 1998. IEEE APCCAS 1998. The 1998 IEEE Asia-Pacific Conference on , 1998
Page(s): 643 -646

[Abstract] [PDF Full-Text (288 KB)] **CNF**

19 **Accumulator based deterministic BIST**
Dorsch, R.; Wunderlich, H.-J.
Test Conference, 1998. Proceedings., International , 1998

Page(s): 412 -421

[Abstract] [PDF Full-Text (652 KB)] **CNF**

20 **Design of a high performance pipelined transversal filter for fading channels equalization**
Wassal, A.G.; Hasan, M.A.
Electrical and Computer Engineering, 1998. IEEE Canadian Conference on , Volume: 1 , 1998
Page(s): 213 -215 vol.1

[Abstract] [PDF Full-Text (292 KB)] **CNF**

21 **The impact of data characteristics and hardware topology on hardware selection for low power DSP**
Keane, G.; Spanier, J.; Woods, R.
Low Power Electronics and Design, 1998. Proceedings. 1998 International Symposium on , 1998
Page(s): 94 -96

[Abstract] [PDF Full-Text (260 KB)] **CNF**

22 **Design and prototyping of DSP custom circuits based on a library of arithmetic components**
Ruiz, P.L.; Riesgo, T.; Uceda, J.
Industrial Electronics, Control and Instrumentation, 1997. IECON 97. 23rd International Conference on , Volume: 1 , 1997
Page(s): 191 -196 vol.1

[Abstract] [PDF Full-Text (548 KB)] **CNF**

23 **VLSI implementation of a 200-MHz 16/spl times/16 left-to-right carry-free multiplier in 0.35 /spl mu/m CMOS technology for next-generation DSPs**
Kolagotla, R.K.; Srinivas, H.R.; Burns, G.F.
Custom Integrated Circuits Conference, 1997., Proceedings of the IEEE 1997 , 1997
Page(s): 469 -472

[Abstract] [PDF Full-Text (364 KB)] **CNF**

24 **A 4.3 ns 0.3 /spl mu/m CMOS 54/spl times/54 b multiplier using precharged pass-transistor logic**
Hanawa, M.; Kaneko, K.; Kawashimo, T.; Maruyama, H.
Solid-State Circuits Conference, 1996. Digest of Technical Papers.

42nd ISSCC., 1996 IEEE International , 1996
Page(s): 364 -365, 474

[Abstract] [PDF Full-Text (1092 KB)] **CNF**

---

25 **General algorithms for reduced-adder integer multiplier design**
Dempster, A.G.; Macleod, M.D.
Electronics Letters , Volume: 31 Issue: 21 , 12 Oct. 1995
Page(s): 1800 -1802

[Abstract] [PDF Full-Text (248 KB)] **JNL**

---

26 **Design methodology for low power data compressors based on a window detector in a 54/spl times/54 bit multiplier**
Song, M.; Asada, K.
Circuits and Systems, 1995. ISCAS '95., 1995 IEEE International Symposium on , Volume: 3 , 1995
Page(s): 1568 -1571 vol.3

[Abstract] [PDF Full-Text (336 KB)] **CNF**

---

27 **A Verilog preprocessor for representing datapath components**
Davis, B.T.; Mudge, T.
Verilog HDL Conference, 1995. Proceedings., 1995 IEEE International , 1995
Page(s): 90 -98

[Abstract] [PDF Full-Text (752 KB)] **CNF**

---

28 **Design strategies for the final adder in a parallel multiplier**
Stelling, P.F.; Oklobdzija, V.
Signals, Systems and Computers, 1995. Conference Record of the Twenty-Ninth Asilomar Conference on , Volume: 1 , 1996
Page(s): 591 -595 vol.1

[Abstract] [PDF Full-Text (488 KB)] **CNF**

---

29 **Hybrid signed-digit number systems: a unified framework for redundant number representations with bounded carry propagation chains**
Phatak, D.S.; Koren, I.
Computers, IEEE Transactions on , Volume: 43 Issue: 8 , Aug. 1994
Page(s): 880 -891

[Abstract] [PDF Full-Text (1148 KB)] **JNL**

30 **An architecture for high-performance/small-area multipliers for use in digital filtering applications**
Kwentus, A.Y.; Hing-Tsun Hung; Willson, A.N., Jr.
Solid-State Circuits, IEEE Journal of , Volume: 29 Issue: 2 , Feb. 1994
Page(s): 117 -121

[Abstract] [PDF Full-Text (580 KB)] **JNL**

[Prev] 1 2 3 4 [Next]

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search
Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting
No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ| Terms | Back to Top

Your search matched **48** of **804507** documents.
Results are shown **15** to a page, sorted by **publication year** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the text box.

Then click **Search Again**.

(multiplier <and> selection <and> adder)

Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

31 **M*N Booth encoded multiplier generator using optimized Wallace trees**
Fadavi-Ardekani, J.
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 1 Issue: 2 , June 1993
Page(s): 120 -125

[Abstract] [PDF Full-Text (424 KB)] **JNL**

32 **Datapath intensive ASIC design-synthesis from VHDL**
Micallef-Trigona, R.
VHDL (Very High Speed Integrated Circuits Hardware Description Language) - Applications and CAE Advances, IEE Colloquium on (Digest No.1993/076) , 1993
Page(s): 4/1 -4/5

[Abstract] [PDF Full-Text (212 KB)] **CNF**

33 **Gate sizing and buffer insertion for optimizing performance in power constrained BiCMOS circuits**
Lowe, K.S.; Gulak, P.G.
Computer-Aided Design, 1993. ICCAD-93. Digest of Technical Papers., 1993 IEEE/ACM International Conference on , 1993
Page(s): 216 -219

[Abstract] [PDF Full-Text (352 KB)] **CNF**

34 **A novel VLSI BiCMOS/bipolar concurrent multiplier-accumulator for DSP applications**

Poornaiah, D.V.; Ananda Mohan, P.; Ahmad, M.O.
Bipolar/BiCOMS Circuits and Technology Meeting, 1993., Proceedings of the 1993 , 1993
Page(s): 171 -174

[Abstract] [PDF Full-Text (480 KB)] **CNF**

---

35 **A graph partitioning problem for multiple-chip design**
Chen, Y.-P.; Wang, T.-C.; Wong, D.F.
Circuits and Systems, 1993., ISCAS '93, 1993 IEEE International Symposium on , May 1993
Page(s): 1778 -1781 vol.3

[Abstract] [PDF Full-Text (312 KB)] **CNF**

---

36 **Design and VLSI implementation of a novel concurrent 16-bit multiplier-accumulator for DSP applications**
Poornaiah, D.V.; Haribabu, R.; Ahmad, M.O.
Acoustics, Speech, and Signal Processing, 1993. ICASSP-93., 1993 IEEE International Conference on , Volume: 1 , 1993
Page(s): 385 -388 vol.1

[Abstract] [PDF Full-Text (296 KB)] **CNF**

---

37 **High-performance/small-area multipliers for use in digital filtering applications**
Kwentus, A.Y.; Hing-Tsun Hung; Willson, A.N., Jr.
Circuits and Systems, 1993., Proceedings of the 36th Midwest Symposium on , 1993
Page(s): 1493 -1496 vol.2

[Abstract] [PDF Full-Text (376 KB)] **CNF**

---

38 **Novel approaches to the design of VLSI RNS multipliers**
Radhakrishnan, D.; Yuan, Y.
Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on , Volume: 39 Issue: 1 , Jan. 1992
Page(s): 52 -57

[Abstract] [PDF Full-Text (536 KB)] **JNL**

---

39 **High speed primitives of hardware accelerators for DSP in GaAs technology**
Sarmiento, R.; Carballo, P.P.; Nunez, A.
Circuits, Devices and Systems, IEE Proceedings G , Volume: 139

Issue: 2 , April 1992
Page(s): 205 -216

[Abstract] [PDF Full-Text (756 KB)] **JNL**

---

40 **Impact of architecture choices on DSP circuits**
Parhi, KK.
TENCON '92. "Technology Enabling Tomorrow : Computers, Communications and Automation towards the 21st Century.' 1992 IEEE Region 10 International Conference. , 1992
Page(s): 784 -788 vol.2

[Abstract] [PDF Full-Text (308 KB)] **CNF**

---

41 **M*N Booth encoded multiplier generator using optimized Wallace trees**
Fadavi-Ardekani, J.
Computer Design: VLSI in Computers and Processors, 1992. ICCD '92. Proceedings, IEEE 1992 International Conference on , 1992
Page(s): 114 -117

[Abstract] [PDF Full-Text (268 KB)] **CNF**

---

42 **A systematic approach for design of digit-serial signal processing architectures**
Parhi, K.K.
Circuits and Systems, IEEE Transactions on , Volume: 38 Issue: 4 , April 1991
Page(s): 358 -375

[Abstract] [PDF Full-Text (1252 KB)] **JNL**

---

43 **A systematic technique for designing highly selective multiplier-free FIR filters**
Saramaki, T.
Circuits and Systems, 1991., IEEE International Sympoisum on , 1991

Page(s): 484 -487 vol.1

[Abstract] [PDF Full-Text (344 KB)] **CNF**

---

44 **Mixed static and domino logic on the CMOS gate forest**
Kernhof, J.; Selzer, M.; Beunder, M.A.; Hoefflinger, B.; Laquai, B.; Schindler, I.
Solid-State Circuits, IEEE Journal of , Volume: 25 Issue: 2 , April 1990

Page(s): 396 -402

[Abstract] [PDF Full-Text (532 KB)] **JNL**

---

45 **A 10 ns 54*54-bit parallel structured full array multiplier with 0.5 mu m CMOS technology**
Mori, J.; Nagamatsu, M.; Hirano, M.; Tanaka, S.; Noda, M.; Toyoshima, Y.; Hashimoto, K.; Hayashida, H.; Maeguchi, K.
VLSI Circuits, 1990. Digest of Technical Papers., 1990 Symposium on , 1990
Page(s): 125 -126

[Abstract] [PDF Full-Text (236 KB)] **CNF**

[Prev] 1 2 3 4 [Next]

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search
Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting
No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ| Terms | Back to Top

Your search matched **48** of **804507** documents.
Results are shown **15** to a page, sorted by **publication year** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the text box.

Then click **Search Again**.

(multiplier <and> selection <and> adder)

Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

46 **Multiplier-free decimator algorithms for superresolution oversampled converters**
Saramaki, T.; Karema, T.; Ritoniemi, T.; Tenhunen, H.
Circuits and Systems, 1990., IEEE International Symposium on , 1990

Page(s): 3275 -3278 vol.4

[Abstract] [PDF Full-Text (340 KB)] **CNF**

47 **BADGE-building block adviser and generator**
Munzner, A.; Pirsch, P.
Circuits and Systems, 1989., IEEE International Symposium on , 1989

Page(s): 1887 -1890 vol.3

[Abstract] [PDF Full-Text (280 KB)] **CNF**

48 **Efficient filtering of images using binomial sequences**
Haddad, R.A.; Nichol, B.G.
Acoustics, Speech, and Signal Processing, 1989. ICASSP-89., 1989 International Conference on , 1989
Page(s): 1590 -1593 vol.3

[Abstract] [PDF Full-Text (228 KB)] **CNF**

[Prev] 1 2 3 4

WEST

Generate Collection | Print

Search Results - Record(s) 1 through 7 of 7 returned.

☐ 1. Document ID: US 5923871 A

L5: Entry 1 of 7 File: USPT Jul 13, 1999

DOCUMENT-IDENTIFIER: US 5923871 A
TITLE: Multifunctional execution unit having independently operable adder and multiplier

Detailed Description Text (31):
Unpack blocks UNPC0 310, UNPC1 312 and UNPC2 314 perform 32-bit operand selection when an operand is read from the register file 130. A double word containing 64-bit data or two 32-bit data words are always read from the register file 130. A first data word is passed unchanged. The position of a second obligatory data word is set by an attribute from the control unit 120. The attribute selects the proper 32 bits of the operand. The 32 selected 32 bits are shifted to the right of the data word.

Detailed Description Text (62):
The multiple function execution unit 800 includes a first input register 830 and a second input register 840 for receiving operands and operation codes from the data multiplexers 143 and unpack circuits 144 shown in FIG. 1. The first input register 830 receives a first operation code OPCODE1 and A and B operands. The second input register receives a second operation code OPCODE2 and a C operand. Operand data and operation codes are applied from the first input register 830 to a bank of three operand buffers 832, 834 and 836 only for simple (noncombined) operations. For combined operations, operand data and operation codes are applied only from the the first input register 830 to a floating-point adder FPA or to a floating-point multiplier FMUL for first-level operations and from the second register 840 for second-level operations.

Detailed Description Text (66):
The selection of operands and operation codes from the buffers 832, 834, 836, 842, 844, and 846 and from the input registers 830 and 840 is controlled by an input control circuit 850 which receives operation codes from the unpack circuits 144. The input control circuit 850 controls multiplexers A 852 and B 854 which select one of the A operands and one of the B operands from the buffers 832, 834, 836 and input register 830. The input control circuit 850 also controls multiplexer OP 856 which selects one of the operation codes from the buffers 832, 834, 836 and input register 830. The input control circuit 850 also controls the multiplexer OP 856 to apply a second operation code from the buffers 842, 844, and 846 and from the input register 840. Accordingly, the input control circuit 850 may control the multiplexer OP 856 to apply either one operation code to both the floating point adder 810 and the floating point multiplier 820 or to apply separate operation codes to the floating point adder 810 and the floating point multiplier 820. For the illustrative circuit, when all first-level operations have a duration of three clocks, the operation code 2 and the operand C for the second-level operation is taken only from the buffer 846. At the same time, the input register 840 and buffers 842 and 844 may store the operation code and the operand C of the combined operation which is started subsequently.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 2. Document ID: US 5870503 A

L5: Entry 2 of 7 File: USPT Feb 9, 1999

DOCUMENT-IDENTIFIER: US 5870503 A
TITLE: Image processing apparatus using error diffusion technique

Detailed Description Text (106):
Image binarization circuit 17 of the sixth embodiment includes, in addition to the first operation loop, a second operation loop including a binary image memory 27 for storing several lines of binarization result g (x, y) (1-bit data of 0 or 1), a binarization average density weighting filter 28 for calculating a binarization result weighting average (binarization average density) Bave.sub.xy of the periphery of the pixel of interest (addition data with respect to the pixel of address (x, y), the same applies hereinafter), a multiplier 29 for applying an operation for carrying out a gamma correction with respect to binarization average error, and a subtractor 30 for calculating the difference between output Bave'.sub.xy from multiplier 29 and the input image data. Subtracted resultant data EBave.sub.xy from subtractor 30 and error weight data Eave.sub.xy from weighting filter 26 are applied to adder 21, so that binarization error is dispersed to peripheral pixels. Thus, the 8-bit continuous tone density data is converted into 1-bit binary data according to the density level by area gradation. The converted 1-bit binary data is printed onto a recording medium by printer 19 (electronic photo printer or ink jet printer).

Detailed Description Text (108):
Referring to FIG. 32, operation panel 12 includes a display 71 for displaying information formed of liquid crystal, a ten key 72 for entering numerics, a start key 73 for initiating operation of reading/copying/printing, a lamp 74 for indicating the operational state, a cursor key 75 for selecting one of the selection branches displayed on information display 71, a function key 76 for selecting one of the three selection branches displayed on display 71, and a reset key 77.

Detailed Description Text (110):
Upon transition to a density adjustment mode on operation panel 12 by the user setting, a density set screen of 9 steps, for example, is shown on display 71 (step S11 in FIG. 33). Simultaneously, "DARK" "AE" and "LIGHT" corresponding to F1-F3 of function key 76 are displayed on the screen. The selection of "DARK" causes the .DELTA. cursor to be shifted one by one leftwards. The gamma characteristic is set so that the output image is darker than the central value. Selection of "LIGHT" causes the .DELTA. cursor to be shifted one by one rightwards. The gamma characteristic is set so that the output image is lighter than the central value. When "AE" is selected, the density will be automatically set to an optimum value according to the original (steps S12-S15).

☐ 3. Document ID: US 5838463 A

L5: Entry 3 of 7 File: USPT Nov 17, 1998

DOCUMENT-IDENTIFIER: US 5838463 A
TITLE: Binary image processor

Detailed Description Text (10):
A threshold generator 35 generates, as the threshold value DT stored in the memory 16 under the control of the CPU 8, a new threshold value THR for the given pixel determined by a pixel clock CKPX and a line clock CKLN generated by the signal controller 14. A binary image determining unit 36 compares the threshold value THR outputted from the threshold generator 35 with a data value EP outputted from the edge emphasis post-processing unit 28 in order to determine the image data of a document as the binary data corresponding to the black and white values of each pixel. In order to effectively control the data output, the data output controller 38 as constructed in accordance with the principles of the present invention receives the shading correction signal SHE outputted from the shading correction controller 22 and the edge emphasis

signal EGE outputted from the edge emphasis controller 24, and generates a latch clock LHCK in response to a data selecting signal DSS supplied from the signal controller 14 under the control of the CPU 8. A data output unit 40 then outputs binary image data determined by the binary image determining unit 36 in accordance with the latch clock LHCK supplied from the data output controller 38 either to the DMA controller 12 when a mode selection signal T/C represents a transmission mode, or alternatively, to the TPH 18 when the mode selection signal T/C represents a copy mode.

Detailed Description Text (15):
FIG. 3 illustrates a detailed circuit diagram of the shading correction and edge emphasis processing unit 100 that comprises the operation unit 20, the shading correction controller 22 and the edge emphasis controller 24 as constructed in accordance with the principles of the present invention. The shading correction controller 22 and the edge emphasis controller 24 are part of the operation control signal generator 51 for generating first to forth operation control signals so as to control the operation unit 20 to execute the shading correction and the edge emphasis of an image. As shown in FIG. 3, the operation unit 20 is composed of a multiplexer 50 for multiplexing between the local mask signal LMK outputted from the edge emphasis mask unit 30 of FIG. 2 and the digital signal ADC outputted from the ADC 6 of FIG. 1, and for generating selected data PB in accordance with the first operation control signal generated by the operation control signal generator 51; an operation selector 60 for performing shift of a given bit for the output data RGO, and for generating shifted data in response to the first operation control signal generated by the operation control signal generator 51 so that the operation unit 20 could operate either as a multi-term adder for edge emphasis, or as a multiplier for shading correction; a first input register 52 for temporarily storing data PA outputted from the operation selector 60 in accordance with a second operation control signal generated by the operation control signal generator 51; a second input register 54 for temporarily storing data PB selected and outputted from the multiplexer 50 in accordance with the third operation control signal generated by the operation control signal generator 51; an adder 56 for adding up the data stored temporarily in the first and second input registers 52 and 54; and an output register 58 for temporarily storing the data added by the adder 56, and for outputting the data RGO in accordance with the fourth operation control signal generated by the operation control signal generator 51.

Detailed Description Text (58):
FIG. 8A illustrates a detailed circuit diagram of the threshold generator 35, and FIG. 8B is a diagram illustrating a 4.times.4 threshold matrix embodied by the circuitry of the threshold generator 35. Referring to FIG. 8A, the threshold generator 35 is composed of four multiplexers 300, 302, 304 and 306 for receiving the threshold data value DT stored previously in the memory 16 by a given line unit in the half-tone process, with the threshold data value DT represented by threshold indexes t.sub.0 .about.t.sub.3, t.sub.4 .about.t.sub.7, t.sub.8 .about.t.sub.11 and t.sub.12 .about.t.sub.15, and for selectively generating one of the received threshold indexes in response to a first selection signal; a multiplexer 308 for selecting a signal outputted from the multiplexers 300, 302, 304 and 306, and for generating the threshold value THR in response to a second selection signal; a first counter 310 for counting in response to the pixel clock CKPX outputted from the signal controller 14 and for generating the first selection signal to the selecting terminals S1 of multiplexers 300, 302, 304 and 306, so as to select a given threshold index of four multiplexers 300, 302, 304 and 306; and a second counter 312 for counting in response to the line clock CKLN outputted from the signal controller 14 shown in FIG. 1 and for generating the second selection signal, so as to select one output from the four multiplexers 300, 302, 304 and 306.

Detailed Description Text (67):
The serial and parallel output units 350 and 352 are exclusively activated by the selection of the mode selecting signal T/C inputted through the I/O interface. A first clock terminals CK1 of the serial and parallel output units 350 and 352 are used to latch the output of the binary image determining unit 36. A second clock terminals CK2 of the serial and parallel output units 350 and 352 are used to generate a copy mode clock CPCK provided to the TPH 18 and a transmission requiring signal TRRQ provided to the DMA controller 12. A signal provided to the first clock terminals CK1 is the latch clock LHCK outputted from the data output controller 38 as shown in FIG. 2. Thus, it can be understood that the latch clock LHCK becomes the shading correction signal SHE and the edge emphasis signal EGE. The delayer 354 delays the latch clock LHCK by 200 nanosecond to produce the delayed latch clock DLHCK to the second clock terminals CK2.

CLAIMS:

1. A binary image processor in an image processing apparatus having an image sensor for reading an image, a converter for converting an electric signal read-out from said image sensor into image data, and a memory for storing a plurality of threshold indexes corresponding to each line unit of said image data, said binary image processor comprising:

threshold generating means for generating a threshold value corresponding to each input pixel of said image data, said threshold generating means comprising first multiplexer means for multiplexing between said plurality of threshold indexes to produce a plurality of discrete values in accordance with a first selection signal, second multiplexer means for multiplexing between said plurality of discrete values to produce said threshold value corresponding to each input pixel of said image data in accordance with a second selection signal, and counter means for counting a pixel clock to produce said first selection signal and counting a line clock to produce said second selection signal;

processing means coupled to receive said image data on a line-by-line basis, for correcting shading and emphasizing edge of said image data to produce processed data having said shading corrected and edge emphasized; and

binarizing means for using half-tone processing to binarize each pixel of said processed data on a basis of said threshold value and generate binary data representing said image.

2. The binary image processor as claimed in claim 1, wherein said first multiplexer means comprises a first multiplexer for multiplexing between a first group of said threshold indexes to produce a first discrete value in accordance with said first selection signal, a second multiplexer for multiplexing between a second group of said threshold indexes to produce a second discrete value in accordance with said first selection signal, a third multiplexer for multiplexing between a third group of said threshold indexes to produce a third discrete value in accordance with said first selection signal, a fourth multiplexer for multiplexing between a fourth group of said threshold indexes to produce a fourth discrete value in accordance with said first selection signal; and said second multiplexer means corresponds to a fifth multiplexer for multiplexing between said first, second, third and fourth discrete values to produce said threshold value in accordance with said second selection signal.

3. The binary image processor as claimed in claim 1, wherein said binarizing means comprises:

a binary image determining unit for making a comparison between each binary bit of said processed data having said shading corrected and said edge emphasized with said threshold value corresponding to said binary bit to determine whether said binary bit represents "black" or "white" pixel, and for generating said binary data representing said image; and

a data output unit for outputting said binary data representing said image for direct printing or distant transmission in response to a mode selection signal.

5. The binary image processor as claimed in claim 3, wherein said data output unit comprises:

a delay for providing a delayed latch clock by delaying a latch clock for a delayed period;

a serial output unit clocked successively by said latch clock and said delayed latch clock, for transmitting said binary data serially to a thermal print head for direct printing when said mode selection signal represents a copy mode; and

a parallel output unit clocked successively by said latch clock and said delayed latch clock, for transmitting said binary data parallel to another binary image processor when said mode selection signal represents a transmission mode.

16. The binary image processor as claimed in claim 15, wherein said threshold generating means further comprises:

means for receiving said plurality of threshold indexes stored in said memory corresponding to each line unit of said image data;

a first counter for counting a pixel clock to produce a first selection signal for controlling individual operation of said plurality of first multiplexers; and

a second counter for counting a line clock to produce a second selection signal to control operation of said second multiplexer.

18. The binary image processor as claimed in claim 17, wherein said edge emphasis mask unit comprises:

means for storing edge emphasis weighting factors and for multiplying each pixel unit of said image data with a corresponding edge emphasis weighting factor to produce a plurality of multiplied data; and

means for making a selection from said plurality of multiplied data and generating said edge emphasis data in response to said third control signal.

25. The binary image processor as claimed in claim 24, wherein said data output means comprises:

delay means for providing a delayed latch clock by delaying a latch clock for a delayed period;

means clocked successively by said latch clock and said delayed latch clock, for transmitting said binary data serially to a thermal print head for direct printing when said mode selection signal represents a copy mode; and

means clocked successively by said latch clock and said delayed latch clock, for transmitting said binary data parallelly to another binary image processor when said mode selection signal represents a transmission mode.

33. The binary image processor as claimed in claim 32, wherein said data output means comprises:

delay means for providing a delayed latch clock by delaying a latch clock for a delayed period;

means clocked successively by said latch clock and said delayed latch clock, for transmitting said binary data serially to a thermal print head for direct printing when a mode selection signal represents a copy mode; and

means clocked successively by said latch clock and said delayed latch clock, for transmitting said binary data in parallel to another binary image processor when said mode selection signal represents a transmission mode.

38. The binary image processor as claimed in claim 37, wherein said data output means comprises:

delay means for providing a delayed latch clock by delaying a latch clock for a delayed period;

means clocked successively by said latch clock and said delayed latch clock, for transmitting said binary data serially to a thermal print head for direct printing when a mode selection signal represents a copy mode; and

means clocked successively by said latch clock and said delayed latch clock, for transmitting said binary data parallelly to another binary image processor when said mode selection signal represents a transmission mode.

☐ 4. Document ID: US 5699459 A

L5: Entry 4 of 7 File: USPT Dec 16, 1997

DOCUMENT-IDENTIFIER: US 5699459 A
TITLE: Image compression device and a method of image compression

Brief Summary Text (20):
In one embodiment of the invention, the image correction section includes: a first pixel value operation section for performing a predetermined operation based on a restored pixel value and at least one of an original pixel value and a corrected pixel value of a reference pixel present in a predetermined position in the processed block and outputting a result of the operation as a first pixel value; a second pixel value operation section for performing a correction process, based on the first pixel value, for an original pixel value of a target pixel present in a predetermined position of the target block corresponding to the reference pixel of the processed block and outputting a second pixel value; and selection means for selecting either the original pixel value of the reference pixel or the second pixel value and outputting the selected pixel value as a corrected pixel value of the target pixel.

Brief Summary Text (24):
In still another embodiment of the invention, the first pixel value operation section is a subtracter for outputting a difference value between the restored pixel value and either the original pixel value or the corrected pixel value of the reference pixel; the first operation section is a multiplier for outputting a multiplied value obtained by multiplying the difference value by the correction coefficient K; the second operation section is an adder for outputting a value obtained by adding the multiplied value to the original pixel value of the target pixel; and the correction coefficient K has a value in the range of $0<K<1$.

Brief Summary Text (29):
In still another embodiment of the invention, the selection section outputs the second pixel value for the target pixel located at the block boundary, the correction process being performed for the target pixel by using the reference pixel, and outputs the original pixel value for any other pixel.

Brief Summary Text (40):
In still another embodiment of the invention, the selection step is a step for outputting the second pixel value for the target pixel located at the block boundary, the correction process being performed for the target pixel by using the reference pixel, and for outputting the original pixel value for any other pixel.

CLAIMS:

2. An image compression device according to claim 1, wherein the image correction means comprises:

first pixel value operation means for performing a predetermined operation based on a restored pixel value and at least one of an original pixel value and a corrected pixel value of a reference pixel present in a predetermined position in the processed block and outputting a result of the operation as a first pixel value;

second pixel value operation means for performing a correction process, based on the first pixel value, for an original pixel value of a target pixel present in a predetermined position of the target block corresponding to the reference pixel of the processed block and outputting a second pixel value; and

selection means for selecting either the original pixel value of the target pixel or the second pixel value and outputting the selected pixel value as a corrected pixel value of the target pixel.

11. An image compression device according to claim 2, wherein the selection means outputs the second pixel value for the target pixel located at the block boundary, the correction process being performed for the target pixel by using the reference pixel, and outputs the original pixel value for any other pixel.

22. A method of image compression according to claim 13, wherein the selection step is a step for outputting the second pixel value for the target pixel located at the block boundary, the correction process being performed for the target pixel by using the reference pixel, and for outputting the original pixel value for any other pixel.

☐ 5. Document ID: US 5119324 A

L5: Entry 5 of 7 File: USPT Jun 2, 1992

DOCUMENT-IDENTIFIER: US 5119324 A
TITLE: Apparatus and method for performing arithmetic functions in a computer system

Brief Summary Text (19):
The adder in the preferred embodiment has a faster core processing speed than the multiplier. Specifically, in the preferred embodiment, the adder has a 25 nanosecond core and the multiplier has a 60 nanosecond core. As one aspect of the present invention, the adder and multiplier are coupled to allow loading of the multiplier with a first and second operand in a first clock cycle of the first clock; performing a first operation in the multiplier core on the first and second operand in a second clock cycle of the first clock; loading the result of the first operation and a third operand in the adder and performing a second operation in the adder in a third clock cycle of the first clock; and unloading the result from the adder in a fourth clock cycle of the first clock.

Detailed Description Text (86):
In a second aspect of the present invention, circuitry is provided to allow an operation in stage 4 914 of the pipeline to utilize data from stage 7 of the pipeline. To facilitate this feature, line 657 is coupled to provide the output data from the adder (unloaded during stage 7) as one input to multiplexors 624-626. This has been termed "short chaining" in the system of the present invention. Selection of a particular input to multiplexors 624-626 is controlled by lines 627-629, respectively.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

☐ 6. Document ID: US 5053986 A

L5: Entry 6 of 7 File: USPT Oct 1, 1991

DOCUMENT-IDENTIFIER: US 5053986 A
TITLE: Circuit for preservation of sign information in operations for comparison of the absolute value of operands

Brief Summary Text (19):
The adder in the preferred embodiment has a faster core processing speed than the multiplier. Specifically, in the preferred embodiment, the adder has a 25 nanosecond core and the multiplier has a 60 nanosecond core. As one aspect of the present invention, the adder and multiplier are coupled to allow loading of the multiplier with a first and second operand in a first clock cycle of the first clock; performing a first operation in the multiplier core on the first and second operand in a second clock cycle of the first clock; loading the result of the first operation and a third operand in the adder and performing a second operation in the adder in a third clock cycle of the first clock; and unloading the result from the adder in a fourth clock cycle of the first clock.

Detailed Description Text (85):
In a second aspect of the present invention, circuitry is provided to allow an operation in stage 4 914 of the pipeline to utilize data from stage 7 of the pipeline. To facilitate this feature, line 657 is coupled to provide the output data from the adder (unloaded during stage 7) as one input to multiplexors 624-626. This has been

termed "short chaining" in the system of the present invention. Selection of a particular input to multiplexors 624-626 is controlled by lines 627-629, respectively.

☐ 7. Document ID: US 4979040 A

L5: Entry 7 of 7 File: USPT Dec 18, 1990

DOCUMENT-IDENTIFIER: US 4979040 A
TITLE: Decoder for subsampled video signal

Detailed Description Text (4):
Line memories 42a-42d each constituting one horizontal scanning period delay circuit operate in response to a clock signal of 16.2 MHz have capacities half those of the one-line memories 24a-24d shown in FIG. 4. One-dimensional transversal filters 43a-43e are different in tap coefficient and circuit configuration from the transversal filters 32a-32e shown in FIG. 4. Delay elements 33h, 33i and 33j in one pixel unit, comprising the D type-FF, operate responsive to the clock signal of 16.2 MHz. The transversal filter 43a comprises a first operation circuit 44 for carrying out a filter operation in response to four successive pixel signals, a second operation circuit 45 for carrying out the filter operation in response to three successive pixel signals, tap coefficient multipliers 34a-34g comprising ROMs, adders 46 and 47, delay elements 48 and 49 in the unit of one pixel, each comprising the D type-FF and operating in response to the clock signal of 16.2 MHz, and switches S4a, S4b and S4c switching for each one horizontal scanning period.

CLAIMS:

5. The pixel signal interpolation device in accordance with claim 1, wherein said timing control means comprises selection means (S4a, S4b, S4c) connected to receive the (m+1) pixel signals delayed from said delay means for selecting the first or latter m pixel signals out of said delayed (m+1) pixel signals in response to the position of said pixel signal to be interpolated; and

said second multiplication means receives said m pixel signals through said selection means.

7. A pixel signal interpolation device (43a) responsive to pixel signals sampled based on interline offset subsampling for interpolating a pixel signal between said sampled pixel signals, comprising:

m (m is an integer of 2 or more) cascaded delay means (33h, 33i, 33j) for delaying said sampled pixel signals in response to a predetermined clock signal;

(m+1) first multiplication means (34a, 34b, 34c, 34d) connected to receive (m+1) pixel signals delayed from said delay means for multiplying each of the (m+1) pixel signals by a predetermined first tap coefficient;

first addition means (46) connected to outputs of said first multiplication means for adding output signals of said first multiplication means;

selection means (S4a, S4b, S4c) connected to receive the (m+1) pixel signals delayed from said delay means for selecting the first or last m pixel signals out of said delayed (m+1) pixel signals in response to a position of said pixel signal to be interpolated;

m second multiplication means (34e, 34f, 34g) connected to outputs of said selection means for multiplying each of the m pixel signals selected by said selection means by a predetermined second tap coefficient;

second addition means (47) connected to outputs of said second multiplication means for adding output signals from said second multiplication means; and

mixing means (S5a) connected to outputs of said first and second addition means for mixing output signals from said first and second addition means in response to said clock signal.

8. The pixel signal interpolation device in accordance with claim 7, wherein said selection means comprises m first switching means (S4a, S4b, S4c) each connected between an input and an output of each of said m delay means for operating responsive to the position of said pixel signal to be interpolated, and

each of said second addition means is connected to an output of each of said first switching means.

11. A MUSE decoder for decoding pixel signals sampled based on Multiple Sub-nyquist Sampling Encoding (MUSE), and alternately receiving pixel signals each constituting at least two frames for forming one picture, said MUSE decoder comprising:

interframe interpolation means (14) for interpolating pixel signals constituting a previous frame between pixel signals constituting a present frame on a horizontal scanning line;

removing means (40) connected to an output of said interframe interpolation means for removing the pixel signals in said previous frame, interpolated by said interframe interpolation means; and

pixel signal interpolation means (43a) connected to an output of said removing means for interpolating pixel signals to be interpolated between the remaining pixel signals in response to the remaining pixel signals in said present frame; wherein

said pixel signal interpolation means comprises

m (m is an integer of 2 or more) cascaded delay means (33h, 33i, 33j) for delaying said remaining pixel signals,

(m+1) first multiplication means (34a, 34b, 34c, 34d) connected to receive (m+1) pixel signals delayed by said delay means for multiplying each of the (m+1) pixel signals by a predetermined first tap coefficient,

first addition means (46) connected to outputs of said first multiplication means for adding output signals of said first multiplication means,

selection means (S4a, S4b, S4c) connected to receive the (m+1) pixel signals delayed by said delay means for selecting the first or latter m pixel signals out of said delayed (m+1) pixel signals in response to positions of said pixel signals to be interpolated,

m second multiplication means (34e, 34f, 34g) connected to outputs of said selection means for multiplying each of the m pixel signals selected by said selection means by a predetermined second tap coefficient,

second addition means (47) connected to outputs of said second multiplication means for adding output signals from said second multiplication means, and

mixing means (S5a) connected to outputs of said first and second addition means for mixing output signals from said first and second addition means in response to said clock signal.

12. The MUSE decoder in accordance with claim 11, wherein said selection means comprises m first switching means (S4a, S4b, s4c) connected between an input and an output of each said m delay means for operating responsive to the positions of said pixel signals to be interpolated, and

each of said second addition means is connected to an output of each of said first switching means.

16. A MUSE decoder for decoding pixel signals sampled based on Multiple Sub-nyquist Sampling Encoding (MUSE), comprising:

distribution means (40, 41, 42a-42d) connected to receive said sampled pixel signals for distributing said sampled pixel signals on n (n is an integer of 2 or more)

horizontal scanning lines constituting one picture; and

n pixel signal interpolation means (43a-43e) connected to each of said distribution means for interpolating pixel signals to be interpolated between the sampled pixel signals on one horizontal scanning line; wherein

said pixel signal interpolation means each comprises

m (m is an integer of 2 or more) cascaded delay means (33h, 33i, 33j) responsive to a predetermined clock signal for delaying the sampled pixel signals distributed by said distribution means,

(m+1) first multiplication means (34a, 34b, 34c, 34d) connected to receive (m+1) pixel signals delayed by said delay means for multiplying each of the (m+1) pixel signals by a predetermined first tap coefficient,

first addition means (46) connected to outputs of said first multiplication means for adding output signals of said first multiplication means,

selection means (S4a, S4b, S4c) connected to receive the (m+1) pixel signals delayed by said delay means for selecting the first or latter m pixel signals out of said delayed (m+1) pixel signals in response to positions of said pixel signals to be interpolated,

m second multiplication means (34e, 34f, 34g) connected to outputs of said selection means for multiplying each of the m pixel signals selected by said selection means by a predetermined second tap coefficient,

second addition means (47) connected to outputs of said second multiplication means for adding output signals from said second multiplication means, and

mixing means (S5a) connected to outputs of said first and second addition means for mixing output signals from said first and second addition means in response to said clock signal.

17. The MUSE decoder in accordance with claim 16, wherein said selection means is further controlled responsive to a position on the horizontal scanning line processed by said pixel signal interpolation means in which said selection means are provided.